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10/825,357	04/16/2004	Dai Yun Lee	8733.1031.00-US	8106
30827 7590 08/10/2010 MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006				
EXAMINER LAM, VINH TANG				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/825,357

**Applicant(s)**

LEE ET AL.

**Examiner**

VINH LAM

**Art Unit**

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 July 2010.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-25 is/are pending in the application.  
4a) Of the above claim(s) 1-3, 6, 24 and 25 is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 4, 5 and 7-23 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 16 April 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO/SB-06)  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_  
Paper No(s)/Mail Date \_\_\_\_\_

## DETAILED ACTION

### *Drawings*

1. The drawing (**FIG. 6**) is objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, “**a control circuit**” (i.e. not the control circuits (**52s**)) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

2. Claims **4** and **19** are objected to because of the following informalities:

Typographical error.

"...wherein the driving circuits **includes...**" should be "...wherein the driving circuits **include...**"

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the **first paragraph** of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims **4** and **19** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding Claims **4** and **19**, the specification as originally filed has failed to provide support for the recitation of "**a control circuit**" that supplies the video signals to the first and second driving circuits, ... and wherein **the control circuit** is positioned

between the first driving circuit the second driving circuit to control the first driving circuit and the second driving circuit". The specification does not reasonably convey one skill in the art how to make or use applicant claimed invention for "a control circuit that supplies the video signals to the first and second driving circuits, ... and wherein the control circuit is positioned between the first driving circuit the second driving circuit to control the first driving circuit and the second driving circuit".

The following is a quotation of the **second paragraph** of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims **4** and **19** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation of Claims **4** and **19** "a control circuit that supplies the video signals to the first and second driving circuits, ... and wherein the control circuit is positioned between the first driving circuit the second driving circuit to control the first driving circuit and the second driving circuit" is not clear.

Does "a control circuit that supplies the video signals to the first and second driving circuits, ... and wherein the control circuit is positioned between the first driving circuit the second driving circuit to control the first driving circuit and the second driving circuit" mean that the **entire display** has **one control circuit**?

According to the Specification's [0067], [0068], and FIG. 6, at least two control circuits (52s) are disclosed.

The above limitation is not only rejected under 35 U.S.C. 112 2<sup>nd</sup> ¶ but also invoked 35 U.S.C. 112 1<sup>st</sup> ¶ since there is no disclosure of "a control circuit that supplies the video signals to the first and second driving circuits, ... and wherein the control circuit is positioned between the first driving circuit the second driving circuit to control the first driving circuit and the second driving circuit" in the originally filed specification.

To further advance prosecution, the Examiner interprets "a control circuit that supplies the video signals to the first and second driving circuits, ... and wherein the control circuit is positioned between the first driving circuit the second driving circuit to control the first driving circuit and the second driving circuit" in agreement with the specification and drawing.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 4-5 and 7-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inukai (US Pub. 2002/0000576) in view of Komiya (US Patent US 6924602).

Regarding Claim 4, (Currently Amended) **Inukai** teaches an electro-luminescence display device, comprising:

electro-luminescence cells ([0070], FIG. 1, i.e. pixel portion 101) arranged in a matrix type ([0075], FIG. 2) at crossings of gate lines ([0074], FIG. 2, i.e.  $G0-G(y+1)$ ) and data lines ([0074], FIG. 2, i.e.  $S1-Sx$ );

a supply voltage line that supplies a driving voltage to the electro-luminescence cells ([0074], FIG. 2, i.e.  $V1-Vx$ );

driving circuits ([0080], [0081], FIG. 3, i.e. 108s for  $G(i \pm n)$  where  $n = 1, 2, 3, \dots$ ) that control a current applied from the driving voltage of the supply voltage line ([0080], [0081], FIG. 3, i.e.  $Vj$ ) to drive the electro-luminescence cells ([0080], FIG. 3) in response to video signals ([0077], FIG. 3, i.e.  $Sj$ ), wherein the driving circuits include[s] a first driving circuit and a second driving circuit ([0080], [0081], FIG. 3, e.g. 108s of  $Gi$  and  $G(i+1)$ ) which are formed at horizontal lines different from each other ([0080], [0081], FIG. 3, e.g. 108s of  $Gi$  and  $G(i+1)$ ).

However, **Inukai** does not teach a control circuit applying video signals to and positioning between the driving circuits.

In the same field of endeavor, **Komiya** teaches

a control circuit (Col. 3, Ln. 53-58, FIG. 1, i.e. comprising TFT1s and TFT4s) that supplies the video signals (Col. 4, Ln. 1-9, FIG. 1, i.e. Data Lines  $n$  where  $n = 1, 2, 3, \dots$ ) to the first and second driving circuits (Col. 3, Ln. 38-44, FIG. 1, i.e. TFT2s top (associated with Gate Line 1) and bottom (associated with Gate Line 2)), is directly connected between the data line (Col. 4, Ln. 1-9, FIG. 1, i.e. TFT1s to Data Line  $n$

where  $n = 1, 2, 3, \dots$ ) and the supply voltage line (Col. 3, Ln. 55-56, FIG. 1, i.e. **TFT4s** to **PVDD**) and is controlled by one of the gate lines (Col. 3, Ln. 44-52, FIG. 1, i.e. **Gate Line  $n$**  where  $n = 1, 2, 3, \dots$ ), and wherein the control circuit is (Col. 3, Ln. 53-58, FIG. 1, i.e. comprising all **TFT1s** and **TFT4s**) positioned between the first driving circuit and the second driving circuit (Col. 3, Ln. 38-44, FIG. 1, i.e. **TFT2s** top (associated with Gate Line 1) and bottom (associated with Gate Line 2)) to control the first driving circuit and the second driving circuit (FIG. 1, i.e. each control circuit supplies video signal independently and correspondingly to the top and bottom driving circuits).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Inukai** teaching of an electro-luminescence display device having gate lines, data lines, a supply voltage line, and driving circuits with **Komiya** teaching of control circuits connections to the driving circuits *to effectively improve the aperture ratio and simultaneously to reduce the power consumption*.

Regarding Claim 19, (Currently Amended) **Inukai** teaches an electro-luminescence display device, comprising:

a plurality of pixels ([0070], FIG. 1, i.e. pixel portion 101) arranged in a matrix type ([0075], FIG. 2);

a plurality of data lines ([0074], FIG. 2, i.e. **S1-Sx**) that applies video signals to the pixels;

a plurality of gate lines ([0074], FIG. 2, i.e. **G0-G(y+1)**) crossing the data lines, electro-luminescence cells provided for each pixel ([0070], FIG. 1, i.e. pixel portion 101);

a supply voltage line that supplies a driving voltage to the electro-luminescence cells ([0074], FIG. 2, i.e.  $V1-Vx$ );

driving circuits ([0080], [0081], FIG. 3, i.e.  $108s$  for  $G(i \pm n)$  where  $n = 1, 2, 3, \dots$ ) that applies a current corresponding to the video signals ([0077], FIG. 3, i.e.  $Sj$ ) to the electro-luminescence cells ([0080], FIG. 3) in response to the video signals ([0077], FIG. 3, i.e.  $Sj$ ), wherein the driving circuits include[s] a first driving circuit and a second driving circuit ([0080], [0081], FIG. 3, e.g.  $108s$  of  $Gi$  and  $G(i+1)$ ) which are formed at horizontal lines different from each other ([0080], [0081], FIG. 3, e.g.  $108s$  of  $Gi$  and  $G(i+1)$ ).

However, Inukai does not teach a control circuit applying video signals to and positioning between the driving circuits.

In the same field of endeavor, Komiya teaches

a control circuit (Col. 3, Ln. 53-58, FIG. 1, i.e. comprising of  $TFT1s$  and  $TFT4s$ ) that supplies the video signals (Col. 4, Ln. 1-9, FIG. 1, i.e. **Data Lines  $n$**  where  $n = 1, 2, 3, \dots$ ) to the first and second driving circuits (Col. 3, Ln. 38-44, FIG. 1, i.e.  $TFT2s$  top (associated with Gate Line 1) and bottom (associated with Gate Line 2)), is directly connected between the data line (Col. 4, Ln. 1-9, FIG. 1, i.e.  $TFT1s$  to **Data Line  $n$**  where  $n = 1, 2, 3, \dots$ ) and the supply voltage line (Col. 3, Ln. 55-56, FIG. 1, i.e.  $TFT4s$  to **PVDD**) and is controlled by one of the gate lines (Col. 3, Ln. 44-52, FIG. 1, i.e. **Gate Line  $n$**  where  $n = 1, 2, 3, \dots$ ), and wherein the control circuit is (Col. 3, Ln. 53-58, FIG. 1, i.e. comprising  $TFT1s$  and  $TFT4s$ ) positioned between the first driving circuit and the second driving circuit (Col. 3, Ln. 38-44, FIG. 1, i.e.  $TFT2s$  top (associated with Gate

*Line 1) and bottom (associated with Gate Line 2)) to control the first driving circuit and the second driving circuit (FIG. 1, i.e. each control circuit supplies video signal independently and correspondingly to the top and bottom driving circuits).*

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Inukai** teaching of an electro-luminescence display device having gate lines, data lines, a supply voltage line, and driving circuits with **Komiya** teaching of control circuits connections to the driving circuits *to effectively improve the aperture ratio and simultaneously to reduce the power consumption.*

Regarding Claim 5, (Previously Presented) the electro-luminescence display device according to claim 4, wherein **Inukai** teaches the first driving circuit is provided at the  $i$ th horizontal line (wherein  $i$  is an integer) to apply the current to the electro-luminescence cell positioned at the  $i$ th horizontal line, in response to a video signal from the control circuit controlled by the  $i$ th gate line, when a gate signal is applied to the  $(i-1)$ th gate line ([0080], [0081], FIG. 3), and

the second driving circuit is provided at the  $(i+1)$ th horizontal line to apply the current to the electro-luminescence cell positioned at the  $(i+1)$ th horizontal line, in response to a video signal from the control circuit controlled by the  $i$ th gate line, when a gate signal is applied to the  $(i+1)$ th gate line ([0080], [0081], FIG. 3).

Regarding Claim 7, (Original) the electro-luminescence display device according to claim 5, wherein **Inukai** teaches the  $(i+1)$ th gate line is connected to a driving circuit provided at the  $(i+2)$ th horizontal line (FIG. 2).

Regarding Claim 8, (Original) the electro-luminescence display device according to claim 5, wherein **Inukai** teaches the (i-1)th gate line ([0080], [0081], FIG. 3)) is connected to a driving circuit provided at the (i-1)th horizontal line ([0080], [0081], FIG. 3).

Regarding Claim 9, (Original) the electro-luminescence display device according to claim 5, wherein **Inukai** teaches the first driving circuits includes:

a first driving thin film transistor having a source terminal connected to the supply voltage line and a drain terminal connected to the electro-luminescence cell positioned at the ith horizontal line ([0082], FIG. 3);

a second driving thin film transistor having a drain terminal connected to a gate terminal of the first driving thin film transistor, a source terminal connected to the control circuit and a gate terminal connected to the (i-1)th gate line ([0080], [0081], FIG. 3); and

a storage capacitor connected between the source terminal and the gate terminal of the first driving thin film transistor ([0081], FIG. 3).

Regarding Claim 10, (Original) the electro-luminescence display device according to claim 5, wherein **Inukai** teaches the second driving circuits includes:

a first driving thin film transistor having a source terminal connected to the supply voltage line and a drain terminal connected to the electro-luminescence cell positioned at the (i+1)th horizontal line ([0080], [0081], FIG. 3);

a second driving thin film transistor having a drain terminal connected to a gate terminal of the first driving thin film transistor, a source terminal connected to the control circuit and a gate terminal connected to the (i+1)th gate line ([0080], [0081], FIG. 3); and

a storage capacitor connected between the source terminal and the gate terminal of the first driving thin film transistor ([0081], FIG. 3).

Regarding Claim 20, (Original) the electro-luminescence display device according to claim 19, **Inukai** further teaches comprising:

a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines ([0124], [0125], FIG. 5A).

Regarding Claim 21, (Original) the electro-luminescence display device according to claim 20, wherein **Inukai** teaches a gate signal applied to the  $i$ th gate line (wherein  $i$  is an integer) overlaps a gate signal applied to the  $(i+1)$ th gate line during one horizontal period ([0124], [0125], FIG. 5A).

Regarding Claim 22, (Original) the electro-luminescence display device according to claim 21, wherein **Inukai** teaches each of the driving circuits includes:

a first driving circuit provided at the  $i$ th horizontal line (wherein  $i$  is an integer) to apply the current to the electro-luminescence cell positioned at the  $i$ th horizontal line, in response to a video signal from the control circuit controlled by the  $i$ th gate line, when a gate signal is applied to the  $(i-1)$ th gate line ([0080], [0081], FIG. 3); and

a second driving circuit provided at the  $(i+1)$ th horizontal line to apply the current to the electro-luminescence cell positioned at the  $(i+1)$ th horizontal line, in response to a video signal from the control circuit controlled by the  $i$ th gate line, when a gate signal is applied to the  $(i+1)$ th gate line ([0080], [0081], FIG. 3).

Regarding Claim 23, (Original) the electro-luminescence display device according to claim 22, wherein **Komiya** teaches one of the control circuits (Col. 3, Ln.

**53-58, FIG. 1, i.e. comprising TFT1s and TFT4s**) is positioned between the first driving circuit and the second driving circuit (*Col. 3, Ln. 38-44, FIG. 1, i.e. TFT2s top (associated with Gate Line 1) and bottom (associated with Gate Line 2)*).

Regarding Claim 11, (Original) the electro-luminescence display device according to claim 9 or 10, wherein **Komiya** teaches the control circuit includes:

a first control thin film transistor having a source terminal connected to the supply voltage line and a drain terminal and a gate terminal connected to the source terminal of the second driving thin film transistor (*Col. 3, Ln. 34-44, FIG. 1*); and

a second control thin film transistor having a drain terminal connected to the gate terminal of the first control thin film transistor, a source terminal connected to the data line and a gate terminal connected to the *i*th gate line (*Col. 3, Ln. 34-44, FIG. 1*).

Regarding Claim 12, (Original) the electro-luminescence display device according to claim 11, wherein **Inukai** teaches any one of the first and second control thin film transistors is provided at the *i*th horizontal line while the remaining control thin film transistor is provided at the (*i*+1)th horizontal line (*[0080], [0081], FIG. 3*).

Regarding Claim 13, (Original) the electro-luminescence display device according to claim 11, **Inukai** further teaches comprising:

a gate driver for applying a gate signal having a turn-on potential during two horizontal periods to the gate lines (*[0124], [0125], FIG. 5A*).

Regarding Claim 14, (Original) the electro-luminescence display device according to claim 13, wherein **Inukai** teaches a gate signal applied to the *i*th gate line

overlaps a gate signal applied to the (i+1)th gate line during one horizontal period ([0124], [0125], FIG. 5A).

Regarding Claim 15, (Original) the electro-luminescence display device according to claim 13, wherein **Inukai** teaches, if a gate signal is applied to the (i-1)th and ith gate lines, then the second driving thin film transistor connected to the (i-1)th gate line and the second control thin film transistor connected to the ith gate line are turned on ([0080], [0081], FIG. 3); and

as the second control thin film transistor is turned on, a video signal from the data line is applied to the first driving thin film transistor and the first control thin film transistor that are positioned at the ith horizontal line ([0080], [0081], FIG. 3).

Regarding Claim 16, (Original) the electro-luminescence display device according to claim 15, wherein **Inukai** teaches the first driving thin film transistor positioned at the ith horizontal line applies the current corresponding to the video signal to the electro-luminescence cell provided at the ith horizontal line ([0080], [0081], FIG. 3).

Regarding Claim 17, (Original) the electro-luminescence display device according to claim 15, wherein **Inukai** teaches the first control thin film transistor applies the current corresponding to the video signal from the supply voltage line to the data line ([0080], [0081], FIG. 3).

Regarding Claim 18, (Original) the electro-luminescence display device according to claim 17, wherein **Inukai** teaches a voltage corresponding to the current

flowing in the first control thin film transistor is stored in the storage capacitor ([0081], FIG. 3).

### ***Response to Arguments/Remarks***

6. Claims 1-3, 6, and 24-25 are canceled.
7. Applicant's arguments filed 07/21/2010 have been fully considered but they are not persuasive.

Applicant argues that Inukai does not teach "driving circuits that control a current applied from the driving voltage of the supply voltage line to drive the electro-luminescence cells in response to video signals, wherein the driving circuits include[s] a first driving circuit and a second driving circuit which are formed at horizontal lines different from each other". However, the examiner respectfully disagree because Inukai teaches the

driving circuits ([0080], [0081], FIG. 3, i.e. 108s for  $G(i \pm n)$  where  $n = 1, 2, 3, \dots$ ) that control a current applied from the driving voltage of the supply voltage line ([0080], [0081], FIG. 3, i.e. Vj) to drive the electro-luminescence cells ([0080], FIG. 3) in response to video signals ([0077], FIG. 3, i.e. Sj), wherein the driving circuits include[s] a first driving circuit and a second driving circuit ([0080], [0081], FIG. 3, e.g. 108s of  $G_i$  and  $G(i+1)$ ) which are formed at horizontal lines different from each other ([0080], [0081], FIG. 3, e.g. 108s of  $G_i$  and  $G(i+1)$ ).

Applicant also argues that **Komiya** does not teach "a control circuit that supplies the video signals to the first and second driving circuits, is directly connected between the data line and the supply voltage line and is controlled by one of the gate lines, and wherein the control circuit is positioned between the first driving circuit and the second driving circuit to control the first driving circuit and the second driving circuit". However, the examiner respectfully disagree because **Inukai** teaches

a control circuit (Col. 3, Ln. 53-58, FIG. 1, i.e. comprising of **TFT1s** and **TFT4s**) that supplies the video signals (Col. 4, Ln. 1-9, FIG. 1, i.e. **Data Lines n** where  $n = 1, 2, 3, \dots$ ) to the first and second driving circuits (Col. 3, Ln. 38-44, FIG. 1, i.e. **TFT2s** top (associated with Gate Line 1) and bottom (associated with Gate Line 2)), is directly connected between the data line (Col. 4, Ln. 1-9, FIG. 1, i.e. **TFT1s** to **Data Line n** where  $n = 1, 2, 3, \dots$ ) and the supply voltage line (Col. 3, Ln. 55-56, FIG. 1, i.e. **TFT4s** to **PVDD**) and is controlled by one of the gate lines (Col. 3, Ln. 44-52, FIG. 1, i.e. **Gate Line n** where  $n = 1, 2, 3, \dots$ ), and wherein the control circuit is (Col. 3, Ln. 53-58, FIG. 1, i.e. comprising **TFT1s** and **TFT4s**) positioned between the first driving circuit and the second driving circuit (Col. 3, Ln. 38-44, FIG. 1, i.e. **TFT2s** top (associated with Gate Line 1) and bottom (associated with Gate Line 2)) to control the first driving circuit and the second driving circuit (FIG. 1, i.e. each control circuit supplies video signal independently and correspondingly to the top and bottom driving circuits).

***Conclusion***

The prior art(s) made of record and not relied upon (is)/are considered pertinent to applicant's disclosure: Fujimoto; Etsuko et al. (US Patent No. 6690034).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH T. LAM whose telephone number is (571)270-3704. The examiner can normally be reached on M-F (7:00-4:30) EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Vinh T Lam/

Examiner, Art Unit 2629

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629